# Neural coding: a perspective for new associative memories

#### Vincent Gripon

Télécom Bretagne

February 26, 2012



Vincent Gripon (Télécom Bretagne)

## Plan

## Introduction

- Challenge
- Approach

#### 2) Our model

- Principle
- Performance
- Application example

#### 3 Direction: learning sequences

## Openings

## Challenge

#### Context

#### Exponential growth of the amount of information



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#### Exponential growth of the amount of information



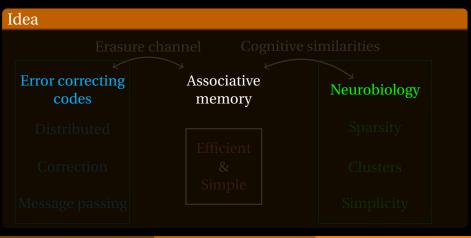
#### Challenge

User	Difficult to find the desired piece of information.
Engineer	Algorithms complexity is limiting, Ad-hoc solutions are often required.

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## Definition

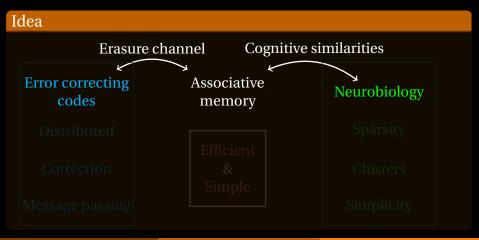
Associative memory = device that can retrieve previously learned messages from part of them.



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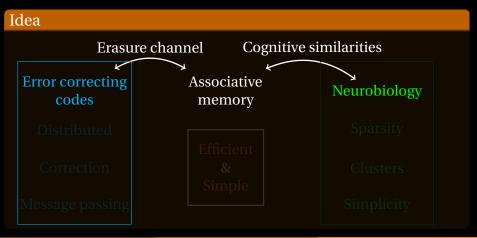
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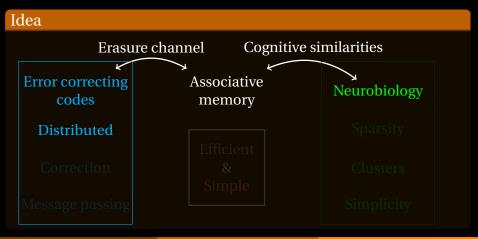
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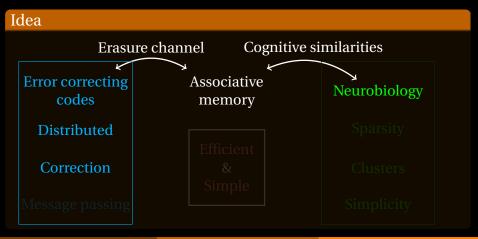
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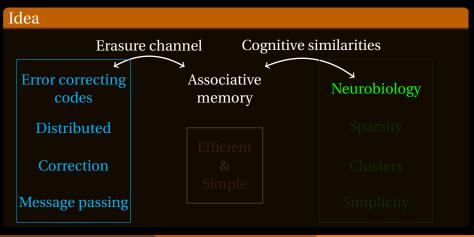
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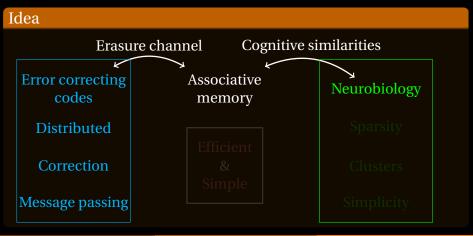
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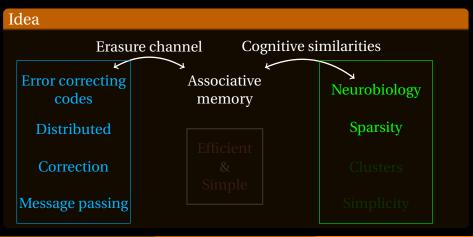
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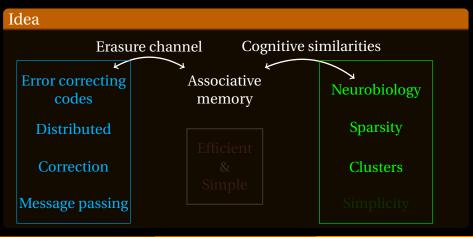
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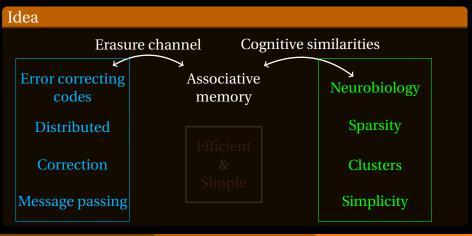
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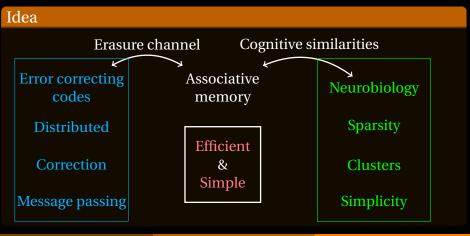
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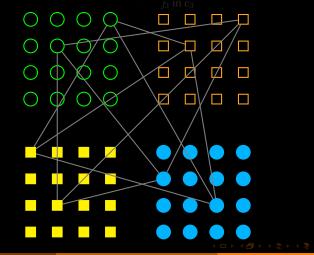
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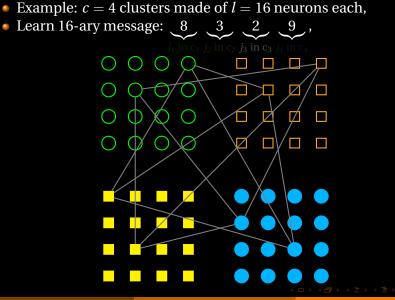
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## Openings

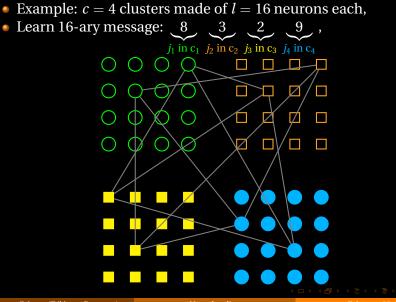
- Example: c = 4 clusters made of l = 16 neurons each,
- Learn 16-ary message:





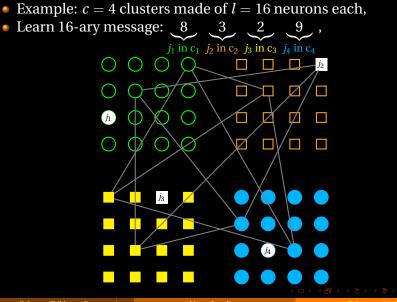
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Neural coding



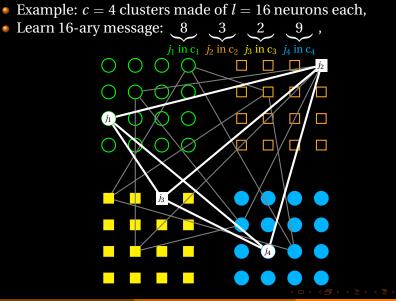
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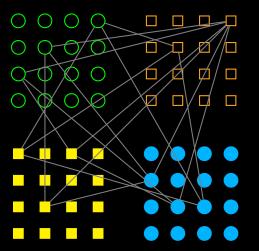
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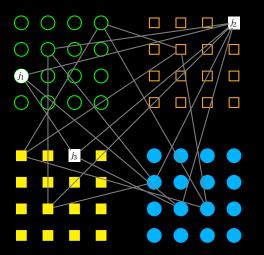




- Projection to the network,
- Global decoding: sum,
- Local decoding: winner-take-all,
- Possibly iterate the two decodings.



 $j_1$  in  $c_1$   $j_2$  in  $c_2$   $j_3$  in  $c_3$ 

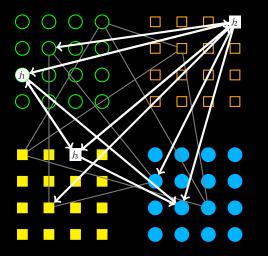


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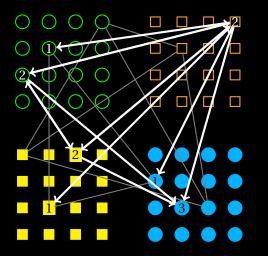


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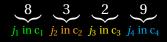
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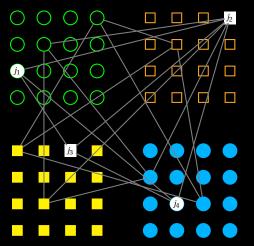


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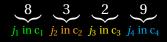


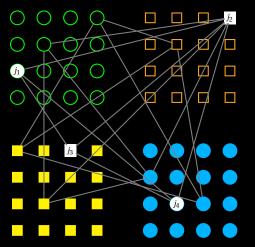
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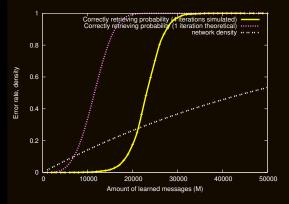




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## Performance

#### Associative memory



c = 8, l = 256 neurons each. Input messages have just 4 known symbols.

State-of-the-art Hopfield network

Our network



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### Role

Speed-up the lookup of frequently accessed data.

#### Context

- With associativity decreases the miss rate,
- Current implementations are limited to 8-ways associativity,
- Speed and area limitations.

- Adaptation of the network:
  - Given the address, find the associated data,
- Additionnal error probability: 10<sup>-30</sup>,
- Area consumption reduced by 65%,
- Pipelined architecture using a few clock cycles.

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## An example: cache design

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### Our proposal

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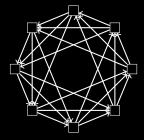
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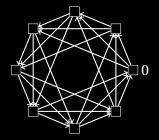
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### Openings

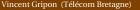


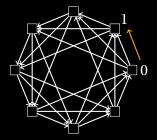
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- *l* = 256 neurons/cluster,
- L = 1000 symbols in sequences,
- *m* = 1823 learned sequences,
- $P_e \leq 0.01$ .





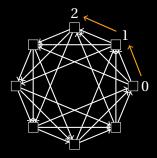
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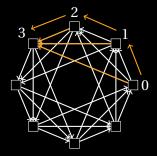
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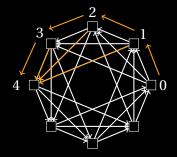
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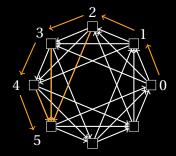
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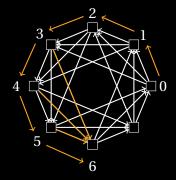
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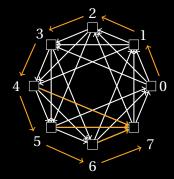
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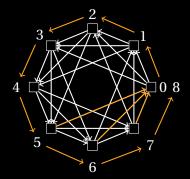
#### February 26, 2012 12 / 15



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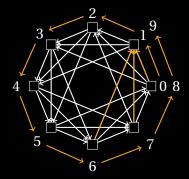
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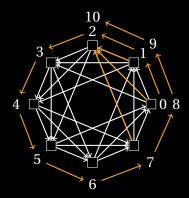
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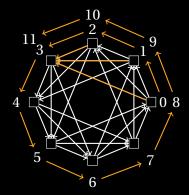
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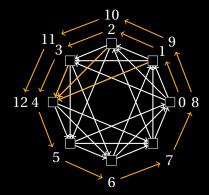
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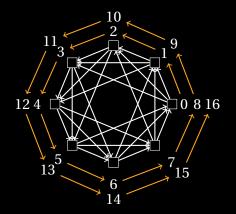
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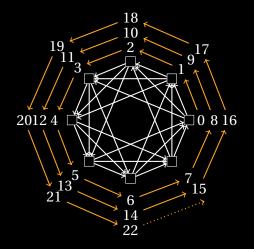
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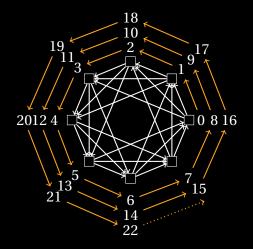
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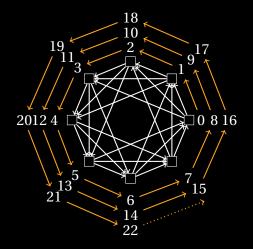
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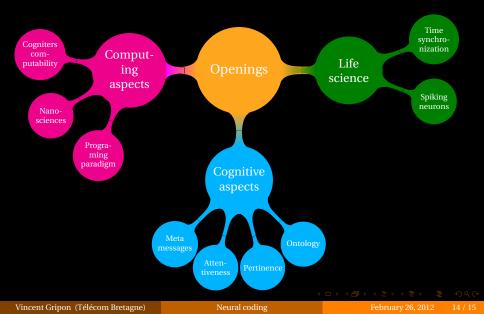
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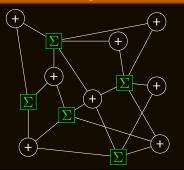


## Openings



# Thank you for your attention. I am at your disposal if you have any question.

### Error correcting code



### Neocortical network

